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SPECIAL ISSUE

DESIGN AUTOMATION OF ELECTRONIC SYSTEMS: PAST ACCOMPLISHMENTS AND CHALLENGES AHEAD

Edited by R. Brayton, L. P. Carloni, A. L. Sangiovanni-Vincentelli, and T. Villa

1958 Boolean Computation Using Self-Sustaining Nonlinear Oscillators
By J. Roychowdhury
|INVITED PAPER| By illustrating the inherent noise-immunity advantages of phase-encoded logic over traditional level-based logic, the author shows how Boolean computation using a wide variety of natural and engineered oscillators becomes possible.

1970 Toeplitz-Plus-Hankel Matrix Recovery for Green's Function Computations on General Substrates
By R. Y. Zhang and J. K. White
|INVITED PAPER| In this paper, the authors show that all elements of an implicitly defined Toeplitz-plus-Hankel (TPH) matrix can be recovered by sampling four or five carefully selected columns, and then using a linear least squares scheme to recover the rest of the matrix.

1985 Progress and Challenges in VLSI Placement Research
By I. L. Markov, J. Hu, and M.-C. Kim
|INVITED PAPER| Extensive research studies performed over the last 50 years addressed numerous aspects of global and detailed placement, a fundamental step in the physical design of integrated circuits. This paper surveys the history of placement research, the progress leading up to the state of the art, and outstanding challenges.

2004 Technology-Dependent Logic Optimization
By R. Murgai
|INVITED PAPER| The survey paper presents the state-of-the-art algorithms for technology-dependent optimizations, along with a comparison of their relative power to optimize the implementations of logic circuits.

2021 Boolean Satisfiability Solvers and Their Applications in Model Checking
By Y. Vizel, G. Weissenbacher, and S. Malik
|INVITED PAPER| This paper traces the important contributions made to modern Boolean satisfiability solvers by the electronic design automation community to address synthesis and verification problems, and discusses its applications in model checking.

2036 Combining Induction, Deduction, and Structure for Verification and Synthesis
By S. A. Seshia
|INVITED PAPER| This paper presents a formal methodology for verification and synthesis that integrates inductive learning with deductive reasoning. A novel theoretical framework is proposed, including the concept of verification by reduction to synthesis, along with examples of practical applications of the methodology.

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DEPARTMENTS

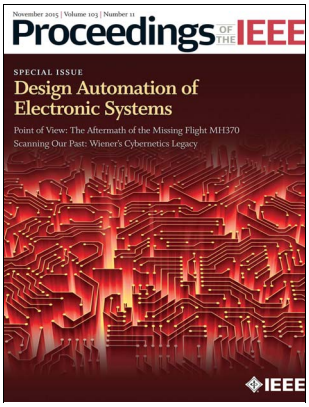
1944 EDITORIAL
By H. J. Trussell and V. Damle

1948 POINT OF VIEW
The Aftermath of the Missing Flight MH370: What Can Engineers Do?
By Y. Yu

1952 SCANNING THE ISSUE
Design Automation of Electronic Systems: Past Accomplishments and Challenges Ahead
By R. Brayton, L. P. Carloni, A. L. Sangiovanni-Vincentelli, and T. Villa

2208 SCANNING OUR PAST
Wiener's Cybernetics Legacy and the Growing Need for the Interdisciplinary Approach
By G. Adamson, R. R. Kline, K. Michael, and M. G. Michael

2215 FUTURE SPECIAL ISSUES/SPECIAL SECTIONS



On the Cover: Our cover this month highlights an electronic circuit layout. Electronic design automation (EDA) offers sophisticated tools to help engineers orchestrate such layouts, whose complexity has been growing over the years.

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SPECIAL ISSUE: Design Automation of Electronic Systems: Past Accomplishments and Challenges Ahead

2052 Toward Unification of Synthesis and Verification in Topologically Constrained Logic Design
By M. Fujita
|INVITED PAPER| In this paper, the author presents a method by which logic synthesis and formal verification can be achieved with a small number of input patterns, if all possible circuit transformations are predetermined.

2061 RTL Synthesis: From Logic Synthesis to Automatic Pipelining
By J. Cortadella, M. Galceran-Oms, M. Kishinevsky, and S. S. Sapatnekar
|INVITED PAPER| The authors review the evolution of RTL synthesis from the early techniques for combinational logic synthesis. Recent methods for automatic pipelining based on elastic timing are then introduced and proposed for microarchitectural exploration.

2076 Application of a Key–Value Paradigm to Logic Factoring
By V. N. Kravets
|INVITED PAPER| The author first revisits a classic algorithm for algebraic factoring to establish a stronger connection to the functional intent rather than to the structural implications of a design description within synthesis, and then presents a scalable factoring algorithm that reduces its dependence on two-level minimization.

2093 System Design Automation: Challenges and Limitations
By J. Sifakis
|INVITED PAPER| This paper discusses to what extent the VLSI-design paradigm can be transposed to hardware/software systems that interact continuously with an external environment, through the application of the principles of separation of concerns, component-based design, semantic coherency, and correctness by construction.

2104 A Platform-Based Design Methodology With Contracts and Related Tools for the Design of Cyber-Physical Systems
By P. Nuzzo, A. L. Sangiovanni-Vincentelli, D. Bresolin, L. Geretti, and T. Villa
|INVITED PAPER| A platform-based design methodology that uses contracts can address the complexity and heterogeneity of cyber–physical systems by providing formal support to the entire system-design flow in a hierarchical and compositional way. The foundations of such flow and the tools supporting its deployment are presented in this paper.

2133 From Latency-Insensitive Design to Communication-Based System-Level Design
By L. P. Carloni
|INVITED PAPER| This paper overviews the principles and practice of latency-insensitive design, offers a retrospective on related research over the past decade, and looks ahead in proposing the protocols and shells paradigm as the foundation to bridge the gap between system-level and logic/physical design, a requisite to cope with the complexity of engineering future system-on-chip platforms.

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2152 Component-Based Design by Solving Language Equations
By T. Villa, A. Petrenko, N. Yevtushenko, A. Mishchenko, and R. Brayton
|INVITED PAPER| The authors review the existing formalisms, algorithmic solutions, and design automation tools to specify and synthesize unknown components in compositional finite-state systems.

2168 New Logic Synthesis as Nanotechnology Enabler
By L. Amarú, P.-E. Gaillardon, S. Mitra, and G. De Micheli
|INVITED PAPER| This paper investigates the relation between logic synthesis and emerging nanotechnologies, and shows how new logic synthesis techniques can enable the identification of the full potential of a given nanotechnology.

2196 A Framework for Genetic Logic Synthesis
By P. Vaidyanathan, B. S. Der, S. Bhatia, N. Roehner, R. Silva, C. A. Voigt, and D. Densmore
|INVITED PAPER| In this paper, the authors introduce a framework to address the challenges of applying logic synthesis techniques to genetic logic devices.